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FPGA PROTOTYPING BY VERILOG EXAMPLES

The value of the d signal is sampled at the rising edge of the clk signal and stored to FF. A D FF may contain an asynchronous reset signal to clear the FF to 0. Its symbol and function table are shown in Figure 4.I(b). Note that the reset operation is independent of the clock signal. FPGA Prototyping b,v Verilog Examples.

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